CLAIMS

We claim:

1. An analog-to-digital (A/D) converter circuit for converting each of a plurality of analog input signals to a plurality of corresponding digital values, comprising:

a comparator having a first input terminal coupled to receive a first signal having a plurality of levels, a second input terminal coupled to receive a plurality of analog input signals, and a third input terminal for receiving a plurality of input select signals, said comparator comprising a multiplexor coupled to a plurality of differential pairs, each differential pair coupled to a respective one of said plurality of analog input signals, said multiplexor selecting one of said plurality of differential pairs based on said plurality of input select signals; and

a latch having a first input terminal coupled to receive an output signal of said comparator, said latch having a data input terminal coupled to receive a series of binary signals, an output signal of said comparator controlling when said latch provides an output signal corresponding to a binary signal applied to said data input terminal,

wherein said comparator compares said first signal with a selected one of said plurality of analog input signals to generate said output signal, and said latch provides one or more bits of an N-bit digital code representing said selected one of said plurality of analog input signals.

2. The circuit of Claim 1 wherein said N-bit digital code comprises one of a Gray code or a thermometer code.

3. The circuit of Claim 1, further comprising:

a first signal generator generating a series of binary codes representing analog levels, said first signal generator further comprising a digital-to-analog converter coupled to receive said binary codes and to generate said first signal being coupled to said first input terminal of said comparator.

4. The circuit of Claim 1 wherein said first signal is an analog ramped signal for each bit of said N-bit digital code.

5. The circuit of Claim 1 wherein said comparator further comprises a current mirror having a first current handling terminal coupled to a first node and a second current handling terminal coupled to a second node, and wherein each of said plurality of differential pairs in said comparator comprises:

a first transistor having a control terminal coupled to receive a respective one of said plurality of analog input signals, a first current handling terminal, and a second current handling terminal coupled to a current source;

a second transistor having a control terminal coupled to receive said first signal, a first current handling terminal, and a second current handling terminal coupled to said current source;

a third transistor having a control terminal coupled to receive a respective one of said plurality of input select signals, a first current handling terminal coupled to said first node, and a second current handling terminal coupled

to said first current handling terminal of said first transistor; and

a fourth transistor having a control terminal coupled to receive said respective one of said plurality of input select signals, a first current handling terminal coupled to said second node, and a second current handling terminal coupled to said first current handling terminal of said second transistor,

wherein said plurality of input select signals selectively enable one of said plurality of differential pairs.

6. The circuit of Claim 5, wherein said comparator further comprises a buffer having an input terminal coupled to said first node for amplifying said output signal of said comparator.

7. The circuit of Claim 6, wherein said buffer comprises a plurality of amplification stages.

8. The circuit of Claim 5, wherein said comparator further comprises:

a plurality of reset transistors, each of said reset transistors having a control terminal coupled to receive a reset signal, a first current handling terminal coupled to said first node, and a second current handling terminal coupled to said control terminal of said first transistor of a respective one of said plurality of differential pairs.

9. The circuit of Claim 8, wherein said reset signal comprises a plurality of reset signals, and each of said control terminals of said plurality of reset transistors is coupled to a respective one of said plurality of reset signals.

10. The circuit of Claim 1, further comprising:

an image sensor formed as an integrated circuit having a plurality of photodetectors, said photodetectors formed within an image sensor array, each of said photodetectors generating an analog signal,

wherein said comparator is one of a plurality of comparators and said latch is one of a plurality of latches all formed within said image sensor array as part of a plurality of analog-to-digital converters, and wherein one comparator and one latch are associated with a group of photodetectors for converting analog signals generated by said group of photodetectors into digital codes, each photodetectors in said group of photodetectors generating one of said plurality of analog input signals.

11. The circuit of claim 10, wherein said one comparator and said one latch are designed into said image sensor array in a symmetrical fashion about said group of photodetectors associated with said comparator and said latch.

12. An analog-to-digital (A/D) converter circuit for converting each of a plurality of analog input signals to a plurality of corresponding digital values, comprising:

a comparator having a first input terminal coupled to receive a first reference signal, a second input terminal coupled to receive a plurality of analog input signals, a third input terminal for receiving a plurality of input select signals, and an output terminal providing an output signal, said comparator comprising a multiplexor coupled to a plurality of differential pairs, each differential pair coupled to a respective one of said plurality of analog

input signals, said multiplexor selecting one of said plurality of differential pairs based on said plurality of input select signals,

wherein said comparator compares said first reference signal with a selected one of said plurality of analog input signals to generate said output signal indicative of one or more bits of an N-bit digital code representing said selected one of said plurality of analog input signals.

13. The circuit of Claim 12 wherein said N-bit digital code comprises a thermometer code.

14. The circuit of Claim 12 wherein said comparator further comprises a current mirror having a first current handling terminal coupled to a first node and a second current handling terminal coupled to a second node, and wherein each of said plurality of differential pairs in said comparator comprises:

a first transistor having a control terminal coupled to receive a respective one of said plurality of analog input signals, a first current handling terminal, and a second current handling terminal coupled to a current source;

a second transistor having a control terminal coupled to receive said first reference signal, a first current handling terminal, and a second current handling terminal coupled to said current source;

a third transistor having a control terminal coupled to receive a respective one of said plurality of input select signals, a first current handling terminal coupled to said first node, and a second current handling terminal coupled to said first current handling terminal of said first transistor; and

a fourth transistor having a control terminal coupled to receive said respective one of said plurality of input select signals, a first current handling terminal coupled to said second node, and a second current handling terminal coupled to said first current handling terminal of said second transistor,

wherein said plurality of input select signals selectively enable one of said plurality of differential pairs.

15. The circuit of Claim 14, wherein said comparator further comprises a buffer having an input terminal coupled to said first node for amplifying said output signal of said comparator.

16. The circuit of Claim 15, wherein said buffer comprises a plurality of amplification stages.

17. The circuit of Claim 14, wherein said comparator further comprises:

a plurality of reset transistors, each of said reset transistors having a control terminal coupled to receive a reset signal, a first current handling terminal coupled to said first node, and a second current handling terminal coupled to said control terminal of said first transistor of a respective one of said plurality of differential pairs.

18. The circuit of Claim 17, wherein said reset signal comprises a plurality of reset signals, and each of said control terminals of said plurality of reset transistors is coupled to a respective one of said plurality of reset signals.

19. The circuit of Claim 14, wherein said current source comprises a fifth transistor having a control terminal coupled to a bias voltage, a first current handling terminal coupled to said second current handling terminal of said first transistor in a respective one of said plurality of differential pairs, and a second current handling terminal coupled to a first reference voltage, wherein said first current handling terminal provides a reference current to each of said plurality of differential pairs.

20. The circuit of Claim 19, wherein said current mirror comprises a sixth transistor and a seventh transistor, control terminals of said sixth and seventh transistors being connected together and to a first current handling terminal of said seventh transistor, a first current handling terminal of said sixth transistor being coupled to said first node, said first current handling terminal of said seventh transistor being coupled to said second node, and second current handling terminals of said sixth and seventh transistors being coupled to a second reference voltage.

21. The circuit of Claim 20, wherein said first, second, third, and fourth transistors comprise NMOS transistors and said sixth and seventh transistors comprise PMOS transistors.

22. The circuit of Claim 21, wherein said first reference voltage comprises a first voltage and said second reference voltage comprises a second positive voltage higher than the first voltage.

23. The circuit of Claim 12, further comprising:

an image sensor formed as an integrated circuit having a plurality of photodetectors, said photodetectors formed within an image sensor array, each of said photodetectors generating an analog signal,

wherein said comparator is one of a plurality of comparators formed within said image sensor array as part of a plurality of analog-to-digital converters, and wherein one comparator is associated with a group of photodetectors for converting analog signals generated by said group of photodetectors into digital codes, each photodetectors in said group of photodetectors generating one of said plurality of analog input signals.

24. The circuit of claim 23, wherein said one comparator is designed into said image sensor array in a symmetrical fashion about said group of photodetectors associated with said comparator.

25. An analog-to-digital (A/D) converter circuit comprising:

a comparator having a first input terminal coupled to receive a first signal having a plurality of levels, a second input terminal coupled to receive said plurality of analog input signals, and a third input terminal for receiving a plurality of input select signals, said comparator including a multiplexor coupling said plurality of analog input signals to a plurality of corresponding input signal paths, said multiplexor selecting one of said plurality of input signal paths based on said plurality of input select signals; and

a latch having a first input terminal coupled to receive an output signal of said comparator, said latch having a data input terminal coupled to receive a series of binary signals, an output signal of said comparator controlling when said latch provides an output signal corresponding to a binary signal applied to said data input terminal,

wherein said comparator compares said first signal with a selected one of said plurality of analog input signals to generate said output signal, and said latch provides one or more bits of an N-bit digital code representing said selected one of said plurality of analog input signals applied to said second input terminal of said comparator; and

wherein said comparator comprises a differential pair and a buffer, said buffer having an input terminal coupled to an output terminal of said differential pair and generating said output signal of said comparator, said differential pair comprising:

a first transistor having a control terminal coupled to receive said first signal, a first current handling terminal coupled to a current mirror, and a second current handling terminal coupled to a current source; and

a first node coupling said plurality of input signal paths to said current mirror, each of said plurality of input signal paths including a second transistor and a third transistor connected in series between said first node and said current source, said second transistor having a control terminal coupled to

a respective one of said input select signal, and said third transistor having a control terminal coupled to a respective one of said plurality of analog input signals, said first node being said output terminal of said differential pair,

wherein said plurality of input select signals selectively enable one of said plurality of input signal paths.

26. The circuit of Claim 25, wherein said buffer comprises a plurality of amplification stages.

27. The circuit of Claim 25, further comprising:

a first signal generator generating a series of binary codes representing analog levels, said first signal generator comprising a digital-to-analog converter connected to receive said binary codes and to generate said first signal being connected to said first input terminal of said comparator.

28. The circuit of Claim 25, further comprising:

a binary signal generator for generating said series of binary signals.

29. An analog-to-digital (A/D) converter circuit for converting each of a plurality of analog input signals to a plurality of corresponding digital values, comprising:

a comparator having a first input terminal coupled to receive a first reference signal, a second input terminal coupled to receive a plurality of analog input signals, a third input terminal for receiving a plurality of input select signals, said comparator including a multiplexor

coupling said plurality of analog input signals to a plurality of corresponding input signal paths, said multiplexor selecting one of said plurality of input signal paths based on said plurality of input select signals,

wherein said comparator compares said first reference signal with a selected one of said plurality of analog input signals to generate said output signal indicative of one or more bits of an N-bit digital code representing said selected one of said plurality of analog input signals.

30. The circuit of Claim 29 wherein said N-bit digital code comprises a thermometer code.

31. The circuit of Claim 29 wherein said comparator comprises a differential pair and a buffer, said buffer having an input terminal coupled to an output terminal of said differential pair and generating said output signal of said comparator, said differential pair comprising:

a first transistor having a control terminal coupled to receive said first reference signal, a first current handling terminal coupled to a current mirror, and a second current handling terminal coupled to a current source; and

a first node coupling said plurality of input signal paths to said current mirror, each of said plurality of input signal paths including a second transistor and a third transistor connected in series between said first node and said current source, said second transistor having a control terminal coupled to a respective one of said input select signal, and said third transistor having a control terminal coupled to a respective one of said plurality of analog

input signals, said first node being said output terminal of said differential pair,

wherein said plurality of input select signals selectively enable one of said plurality of input signal paths.

32. The circuit of Claim 31, wherein said buffer comprises a plurality of amplification stages.

33. A method for performing analog-to-digital conversion comprising:

receiving a first analog signal having a plurality of levels;

receiving a plurality of analog input signals each to be converted into a digital value;

coupling said plurality of analog input signals to a corresponding plurality of differential pairs in a comparator;

selecting one of said plurality of differential pairs based on a plurality of input select signals;

comparing said first analog signal to a selected analog input signal associated with said selected one of said plurality of input signal paths, and outputting a comparison result;

receiving a series of binary signals; and

applying said comparison result to a first input of a latch, and applying said series of binary signals to a data input of said latch, a logic level of said comparison result controlling when said latch provides an output signal corresponding to a binary signal applied to said data input,

wherein said latch provides one or more bits of an N-bit digital code representing at least one of said analog input signals.

34. A method for performing analog-to-digital conversion comprising:

receiving a first reference signal corresponding to a plurality of decrementing digital count values;

receiving a plurality of analog input signals each to be converted into a digital value;

coupling said plurality of analog input signals to a corresponding plurality of differential pairs in a comparator;

selecting one of said plurality of differential pairs based on a plurality of input select signals;

comparing said first reference signal to a selected analog input signal associated with said selected one of said plurality of input signal paths, and outputting a comparison result; and

applying said comparison result to a buffer,

wherein said buffer provides one or more bits of an N-bit digital code representing at least one of said analog input signals.